REMARKS/ARGUMENTS

Claims 1-38 are pending in this application. Claims 4-11, 15-22 and 34-37 have been allowed. Claims 1-3, 23 and 30-33 stand rejected. The Examiner continues to reject claims 1-3, 23 and 30-33 based upon the Osborn et al. reference. The Examiner says that Osborn et al. state at column 5, lines 57-60 that their circuit compensates for temperature changes, i.e., both overtemperature and undertemperature conditions. In other words, the Examiner states, in Osborn et al., if there is an overtemperature condition, the feedback will cause the output of comparator 230 to change thus keeping load current IL from undesirably going up or down. The Examiner indicates that this feedback control is a type of "protection" even though Osborn et al. do not call it protection per se. The Examiner further argues that the protection signal of the present invention is not doing any protecting itself, that it is only an indication of when the temperature has risen, i.e., Applicants do not show what to do with the overtemperature protection signal.

Addressing the Examiner's comments, Applicants do concede that the feedback loop of the Osborn et al. circuit will cause the output of the comparator 230 to change thus keeping the target current ratio of IL to I sense maintained and thus the circuit 200 of Osborn et al. is operable to control the load current. See column 7, lines 50-53. However, that being said, Osborn et al. fail to teach or suggest a comparator that generates an overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs. Osborn et al. may generate a signal that is dependent on temperature changes. However, it does not produce an overtemperature protection signal. Applicants have amended claims 1 and 30 to recite that the comparator generates the overtemperature protection signal when the temperature of the power MOS device has exceeded a predetermined level determined by the predetermined inequality. There is no teaching or suggestion in Osborn of generating such an overtemperature protection signal when the temperature of the power MOS device exceeds a predetermined level. For example, this is shown in Fig. 2A of the present application for the circuit of Fig. 2 wherein the overtemperature protection signal is generated when the temperature exceeds 160°C. There is no teaching or suggestion in Osborn of generating such an overtemperature protection signal even if the output of Osborn's comparator

230 does depend on temperature. Ostorn et al do not show or suggest how to design a circuit that provides such an overtemperature protection signal that is generated at a predetermined temperature based upon the inputs to the comparator. Osborn's circuit simply changes based on temperature. It does not produce an overtemperature protection signal at a predetermined temperature, as now claimed.

Secondly, addressing the Examiner's second point that the Applicants do not show what to do with the overtemperature protection signal. Applicants disagree. Clearly, Applicants' overtemperature protection signal is exactly that. It is a signal which indicates that a certain temperature has been exceeded. A person of skill in the art would use that signal to turn off the power MOS device and thus remove or limit the current to the load. That is the point of the device. In fact, Applicants do disclose a protection scheme. The protection scheme is that if the overtemperature protection signal is generated, the MOSFET device can be turned off or the current limited to protect it. Clearly this is the intent of Applicants' invention. In the Background of the Invention, Applicants state at page 1, line 18 that in order to prevent damage to power semi-conductor devices, "the maximum operating temperature of the devices should not be exceeded." Applicants continue that it is "important to monitor the temperature of power semiconductor devices so that they can be shut down or the current limited through them if the maximum operating temperature is reached in order to prevent damage to the devices." Accordingly, Applicants do describe a scheme for protecting the devices. Once the overtemperature protection indication is generated, the MOSFET is shut down, or the current is limited.

Applicants accordingly submit that in view of the amendments, this application, including all rejected claims together with the claims that have been withdrawn from issue (which should be rejoined), should now be allowed.

An amendment to the specification has also been made on page 2, where claim 1 should have been inserted in the summary.

In view of the above, a Notice of Allowance is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 8, 2005.

Louis C. Dujmich
Name of applicant, assignee or Registered Representative

Signature

March 8, 2005
Date of Signature

LCD/jh

Respectfully submitted,

Louis C. Dujmich
Registration No.: 30,625
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700